AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for selective electroplating of a semiconductor input/output (I/O) pad, the method comprising:

forming a titanium-tungsten (TiW) layer over a passivation layer on a semiconductor substrate, said TiW layer further extending into an opening formed in said passivation layer for exposing the I/O pad, such that said TiW layer covers sidewalls of said opening and a top surface of the I/O pad;

forming a seed layer over said TiW layer;

selectively removing portions of said seed layer such that remaining seed layer material corresponds to a desired location of interconnect metallurgy for the I/O pad; and

electroplating at least one metal layer over said remaining seed layer material, and thereby encapsulating exposed outer sidewalls thereof with respect to said TiW layer, using said TiW layer as a conductive electroplating medium, wherein said electroplating is implemented ~~in the absence of a photolithographically formed masking~~ layer without a photoresist present during the electroplating step.

2. (previously presented) The method of claim 1, wherein said seed layer further comprises a Cu over CrCu layer.

3. (original) The method of claim 1, wherein said at least one metal layer further comprises a nickel layer followed by a gold layer.

4. (original) The method of claim 1, further comprising removing portions of said TiW layer not covered by said at least one metal layer following electroplating thereof.

5. (original) The method of claim 1, wherein the I/O pad further comprises an

PAGE 4/9 * RCVD AT 3/17/2006 2:47:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/6 * DNIS:2738300 * CSID:8602860115 * DURATION (mm-ss):02-46

aluminum pad.

6. (original) The method of claim 1, wherein said seed layer is selectively removed by photoresist patterning.

7. (original) The method of claim 1, wherein said passivation layer further comprises a photosensitive polyimide (PSPI) layer.

8. (withdrawn) A semiconductor input/output (I/O) pad structure, comprising:

a titanium-tungsten (TiW) layer formed into an opening formed in a passivation layer on a semiconductor substrate, said opening created for exposing an I/O pad, such that said TiW layer further covers sidewalls of said opening and a top surface of said I/O pad;

a seed layer formed over a portion of said TiW layer and corresponding to a desired location of interconnect metallurgy for said I/O pad; and

at least one metal layer electroplated over said seed layer, wherein said TiW layer serves as a conductive electroplating medium.

9. (withdrawn) The I/O pad structure of claim 8, wherein said seed layer further comprises a Cu/CrCu layer.

10. (withdrawn) The I/O pad structure of claim 8, wherein said at least one metal layer further comprises a nickel layer followed by a gold layer.

11. (withdrawn) The I/O pad structure of claim 8, wherein said I/O pad further comprises an aluminum pad.

12. (withdrawn) The I/O pad structure of claim 8, wherein said at least one metal layer partially encapsulates a sidewall of said seed layer.

PAGE 5/9 * RCVD AT 3/17/2006 2:47:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/6 * DNIS:2738300 * CSID:8602860115 * DURATION (mm-ss):02-46

13. (withdrawn) The method of claim 12, wherein said at least one metal layer covers a remaining portion of said TiW layer not covered by said seed layer.

14. (withdrawn) The method of claim 8, wherein said passivation layer further comprises a photosensitive polyimide (PSPI) layer.

PAGE 6/9 * RCVD AT 3/17/2006 2:47:33 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/6 * DNIS:2738300 * CSID:8602860115 * DURATION (mm-ss):02-46